SoC architecture tackles industrial networking

By Kyle Harper

Finally, the network is *the microprocessor. Our coverage of the latest in System-on-Chip (SoC) technology starts with a look at key points of an industrial SoC architecture and features designed for industrial control networks in an integrated device. Kyle highlights flexible memory architecture, the integrated IEEE 1588 timing protocol, and a configurable timing block.*

A revolution is quietly overtaking the industrial and general-purpose microcontroller (MCU) markets. Indeed, networking has found its way into even the most deeply embedded devices in the industrial, scientific, and commercial market segments. What was once the exclusive domain of 8-bit and 16-bit MCUs performing only a few tasks embedded in isolated equipment is now a field of applications calling for higher-performing 32-bit SoCs to handle the additional network connectivity tasks.

A new class of SoC architecture is emerging, one that fits the new challenges for an industrial networking device. These challenges include scalable data and I/O processing, synchronized networking, and configurable timing.

Scalable data and I/O processing

Traditional sub-100 MHz 32-bit RISC-based and DSP-based MCUs, burdened with their slow on-chip buses and flash, tend to struggle under this new additional connectivity workload. Even if these traditional flash-based MCUs can be pushed to higher clock speeds, the on-chip flash and narrow 32-bit buses do not scale – the application simply *waits faster* with little real data and I/O throughput improvement.

An SoC built for data and I/O traffic should have both a high-performance processor and busing capable of handling the heavy DMA I/O traffic that typically occurs in demanding embedded and industrial applications, which now require connectivity. DMA should be optimized to not interfere with core processor operations.

Ideally, an SoC architecture would scale, enabling single-chip solutions using on-chip memory, or multichip solutions with additional external memory. Using on-chip SRAM instead of traditional flash would help increase performance, lower power, and reduce cost. Similarly, supporting external Pseudo Static RAMs (PSRAMs) and CellularRAM (low-power and bursting RAM products already used pervasively in mobile markets) would enable system designers to cost effectively scale memory solutions, allowing a single SoC architecture to service a range of designs.

PSRAMs and CellularRAMs

Pseudo Static RAMs (PSRAMs) generally combine the features of DRAM and SRAM to create higher-density, lower-power devices. CellularRAM, the trademark name for Micron's PSRAM device with an asynchronous/page and burst flash interface, offers compatibility with flash interfaces, higher data throughput, and low active and standby current levels compared to DRAM devices. Learn more at www.cellularram.com.

In sync with networking

Key connectivity peripherals for an industrial networking SoC include Ethernet, USB, and CAN, enabling designers to build flexible networking gateways. Directly integrating these peripherals with elements such as A/D and D/A converters and timers in an SoC device for industrial applications is a given.

A new standard building momentum is the IEEE 1588 Precision Timing Protocol (PTP). An IEEE 1588 controller provides precise, hard, real-time control, trigger, and time stamping of Ethernet packets and I/O events. IEEE 1588 is rapidly gaining popularity as an open standard synchronization protocol for *taming* Ethernet and TCP/IP for use in precisely synchronizing events (for example, sensor capture and task and event triggering) among literally thousands of devices deployed across any LAN hierarchy.

IEEE 1588 applies not just in the industrial market that initiated this IEEE standard, but in any market segment needing cost-effective network synchronization and event triggering.

Timing is everything

Traditional timer controllers are architected and hardwired by a chip designer to a particular preconceived notion of how a timer should be built and used in a particular application. Configurable timer blocks, on the other hand, allow system designers to mimic virtually any type of existing timer architecture or create their own custom mix of timer elements.

IEEE 1588 protocol in brief

The basic function of IEEE 1588 is that the most precise clock on the network synchronizes all other users. A clock with only one network port is termed an *ordinary clock.* There are two clock classes, master and slave. In principle, any clock can perform both the master and slave function.

The precision of a clock is categorized by the protocol in terms of classes (stratum). For example, the protocol may determine that the highest precision clock happens to be an atomic clock, thus will assign this clock source as *master clock* with a stratum value *1*. All other clocks will be assigned as *slave clocks* with various lower stratum values. The selection of the best clock in the network is performed automatically using the protocol's *best master clock* algorithm.

The precision of the synchronization depends heavily on the network and the components used in the network. For this reason, the transition over less deterministic components, such as routers and switches, is also made as precise as possible for the protocol using what is called a *boundary clock.*

A management protocol is available for the administration and configuration of clocks in the network.

The IEEE 1588 Precision Timing Protocol (PTP) is based on IP multicast communication and is not restricted to Ethernet, but can be used on any bus system that supports multicasting. Multicast communication offers the advantage of simplicity; IP address administration does not need to be implemented on the PTP nodes. Furthermore, PTP can be scaled for a large number of PTP nodes.

Learn more at www.ieee1588.com.

A timer block should enable system designers to construct complex timing functions requiring deterministic behavior without resorting to specialized complex scripting or DSP programming languages (and hard-to-find specialized expertise). It should offload the CPU and software significantly in even the most complex timing algorithms, thus freeing up the CPU and bus bandwidth for use elsewhere in the application. A few examples of these complex real-time functions in industrial applications include:

- Pulse Width Modulation (PWM) and space vector PWM functions with nonoverlap times
- Quadrature encoder sensing and control
- Programmable *deadband* intervals
- Pulse period measurement
- 48-bit input capture function
- 48-bit output compare function

Also, these timers should coordinate with the IEEE 1588 PTP network clock, allowing the system designer to time-stamp and trigger events across an entire IEEE 1588 PTP network of nodes. This architecture synchronizes nodes simply, precisely, and accurately without CPU, software, and interrupts involved in the critical path, thus avoiding synchronization jitter.

Architecture meets silicon

These architectural points are implemented in the AMCC PPC405EZ, an easily programmable general-purpose PowerPC 405-based microprocessor that offers an ideal upgrade path for applications with 8-bit, 16-bit, RISC, or DSP MCUs needing a performance and connectivity upgrade. Figure 1 shows a block diagram of the device.

The PPC405EZ uses a PowerPC 405 RISC CPU core with a 166 MHz 64-bit processor local bus and a 83 MHz 32-bit on-chip peripheral bus. The 83 MHz 16-/32-bit external bus provides bus arbitration for multimaster shared RAM system designs. The 32 kB SRAM on-chip memory stores critical instructions and data, providing fast access for processing- and data-intensive algorithms. All on-chip DMAs can access this on-chip memory. External memories supported include SRAM, PSRAMs, CellularRAMs, ROM, NOR and NAND flash, as well as SPI- or I2C-based NVRAMs. Indeed, it is possible to build a complete high-performance embedded solution with just the on-chip 32 kB SRAM plus one NVRAM device (NOR, NAND, SPI, or I2C). Systems ranging from simple to multimaster configurations can be built.

The PPC405EZ's connectivity package consists of one Fast Ethernet port with an integrated IEEE 1588 PTP controller, three USB 1.1/2.0 Full Speed compatible ports with integrated PHYs, and two CAN 2.0b ports. Features include one 8-input 10-bit 300 kSps ADC, one 10-bit 30 MSps DAC, and a configurable auto-reloading 15-channel Chameleon Timer/PWM controller that significantly offloads the CPU and software for complex timing and waveform generation. The IEEE 1588 PTP controller is fully integrated directly into the analog functions, the Chameleon Timer, and other on-chip functions to optimize performance and eliminate CPU involvement in capturing, triggering, and time-stamping deterministic real-time events in devices that are local or deployed across entire networks.

Tighter event control

With this type of architecture, gone are the days when a system designer/programmer would struggle with synchronizing just a few real-time I/O events across a single chip or even across a single board, let alone I/O events across an entire network. Using an architecture optimized for networking – delivering

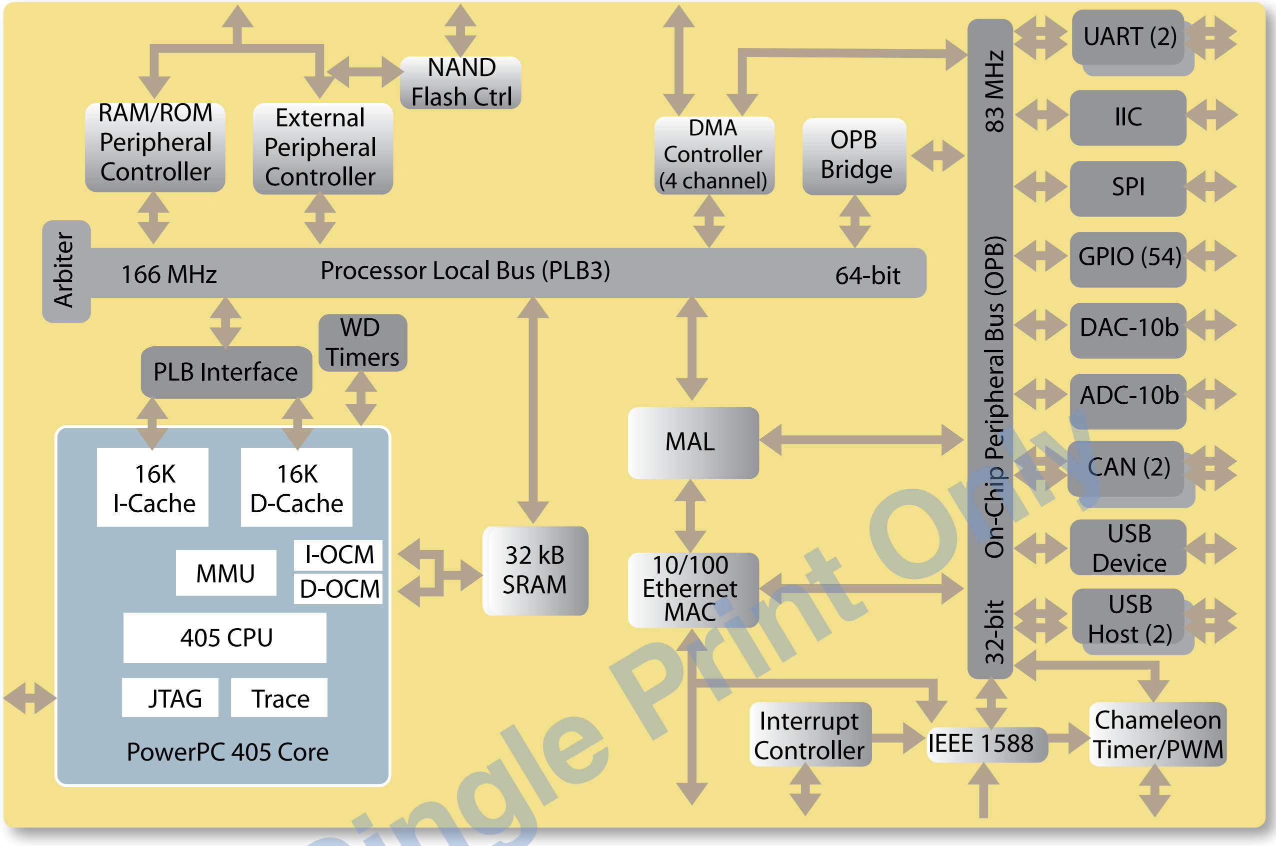

Figure 1

scalable data and I/O processing, synchronized networking, and configurable timing – designers can control tightly synchronized I/O events across an entire network of devices. IES

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